Abstract

In an adaptive equalizer circuit, to an input having a fluctuating amplitude, a stable adaptive equalization operation can be realized without changing over a reference value for computing an equalization error. An input signal is held as a sample with a timing signal shifted from a reference clock of the input signal by a phase of 1/2 cycle. An equalization output is computed from an obtained sample data. The difference between only the first output value after a zero-crossing and an arbitrary set reference value is computed and the computed value is set as an equalization error. A coefficient of the adaptive equalization circuit is updated from the equalization error and the sample data. Further, to the displacement of the symmetry of the input signal, the reference value of the adaptive equalizer circuit is changed corresponding to the change of a binarization threshold value of a binarization circuit which constitutes a rear stage of the adaptive equalizer circuit.